

Figure 1 Packet rate vs. packet size

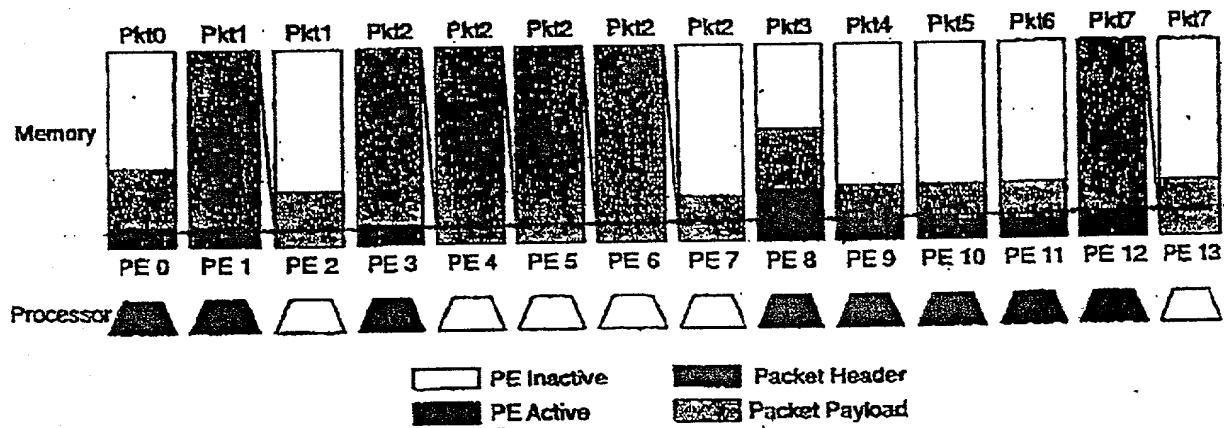


Figure 2 Allocation of packets to Processing Elements

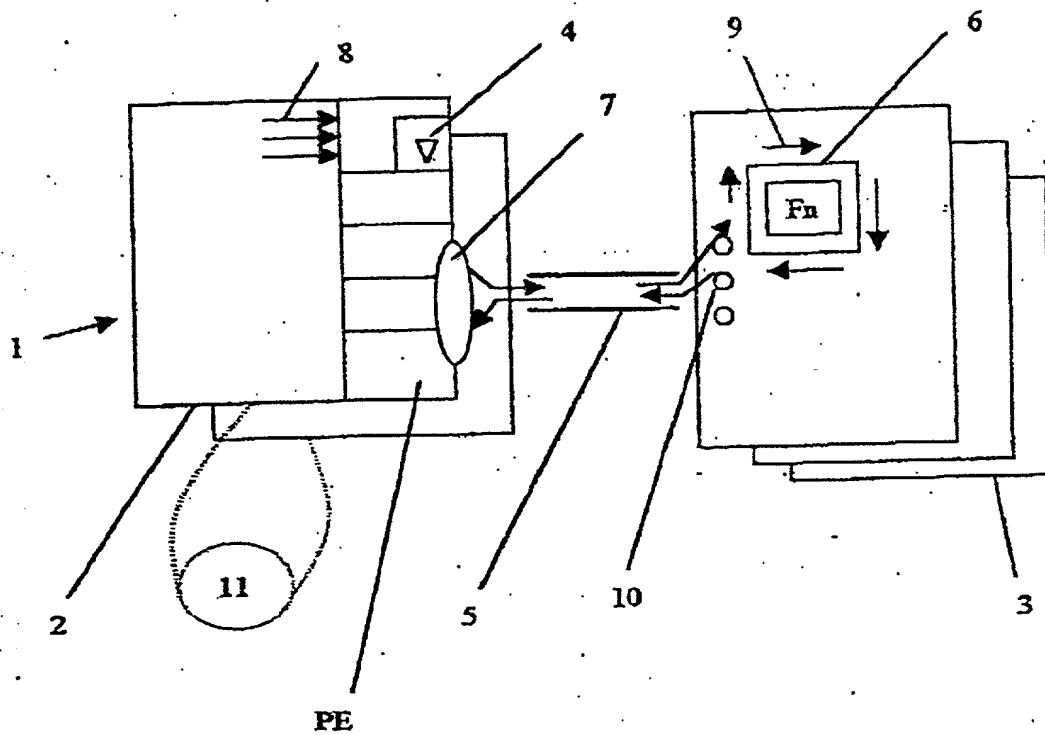


Figure 3

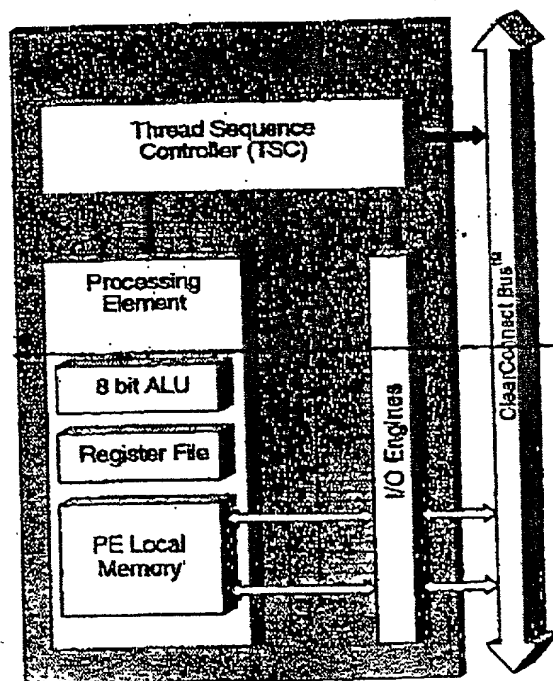


Figure 4 Structure of MTAP processor.

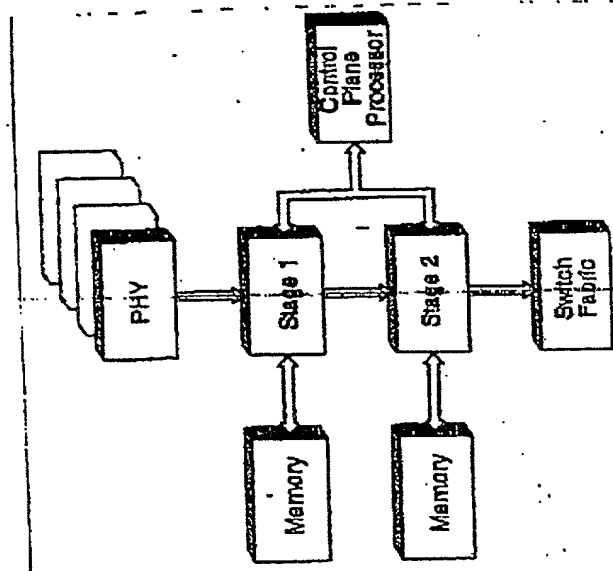
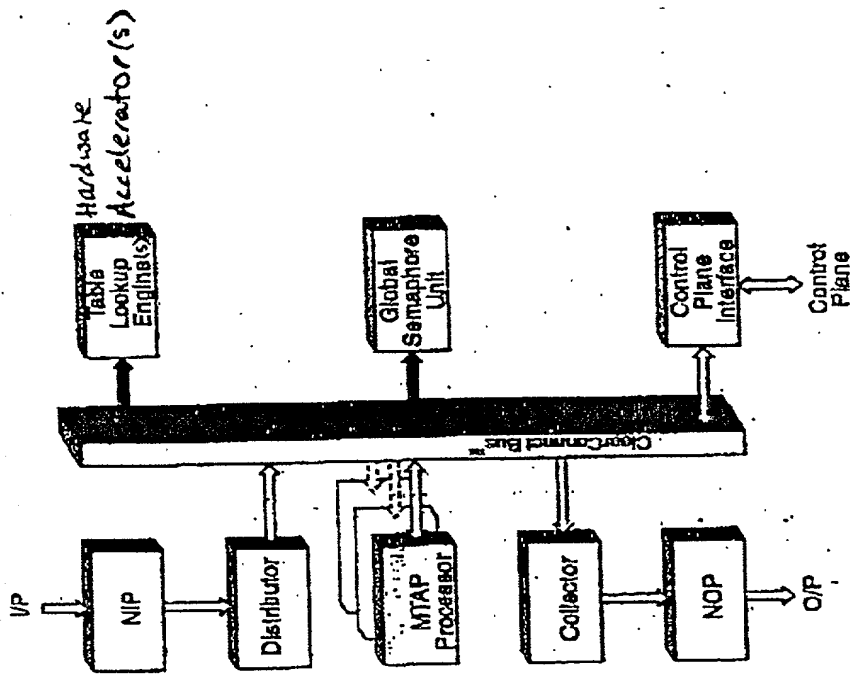


Figure 5 Example Ingress pipeline



Key:
 ⇄ Fast path packet flows
 ⇨ Fast path control flows

Figure 6 Example fast path processing subsystem

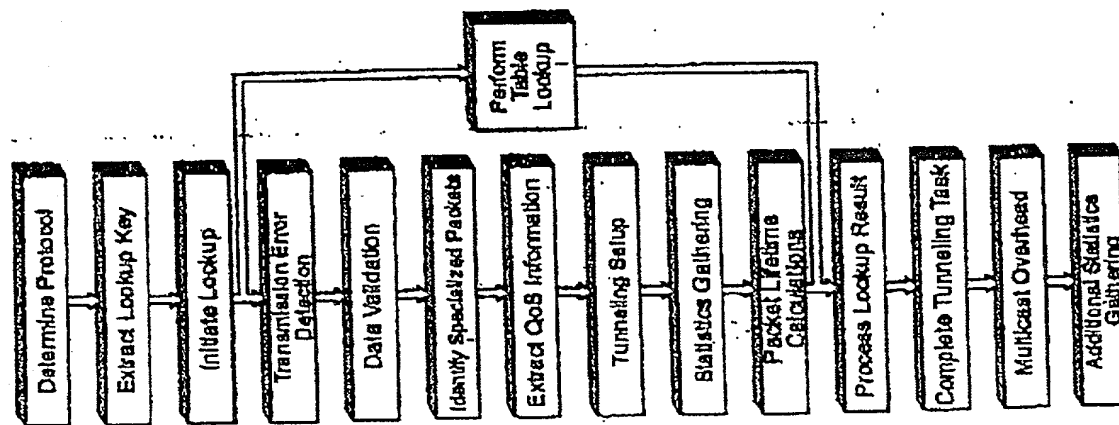


Figure 8 Overview of packet processing and table lookup

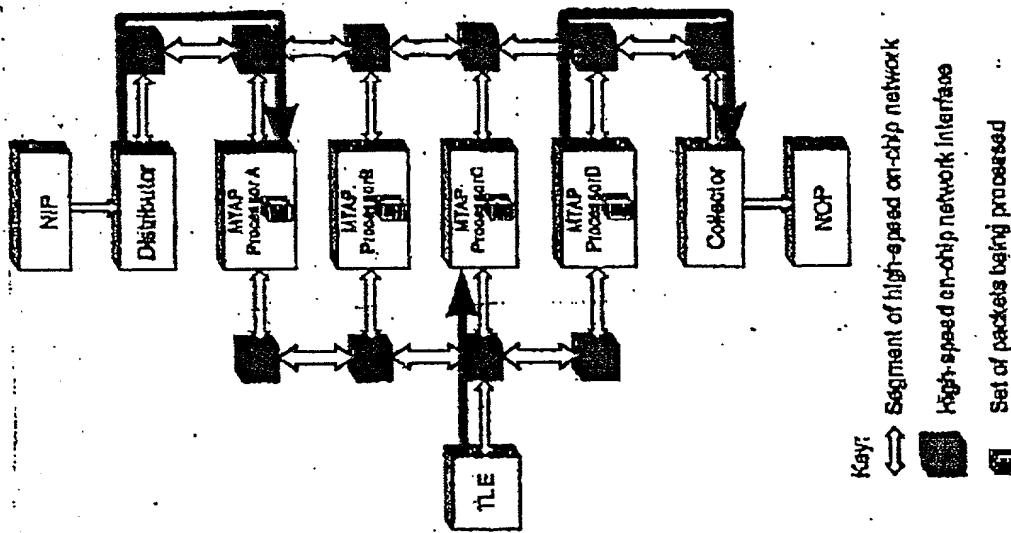


Figure 9 Snapshot of system behavior

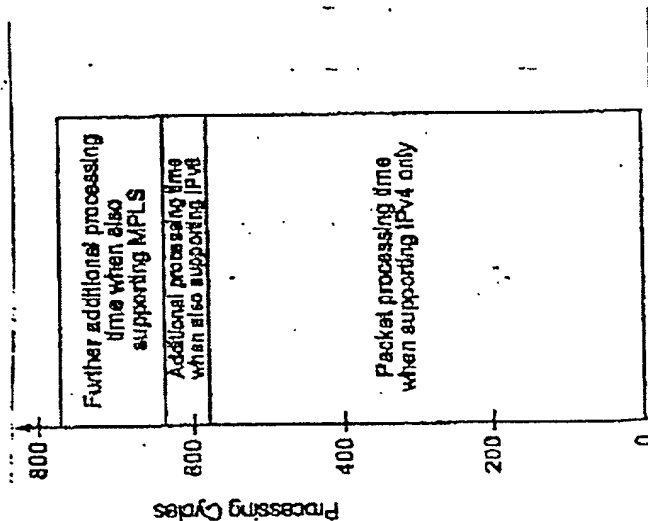


Figure 6 Cycle expenditure for multiple protocol support

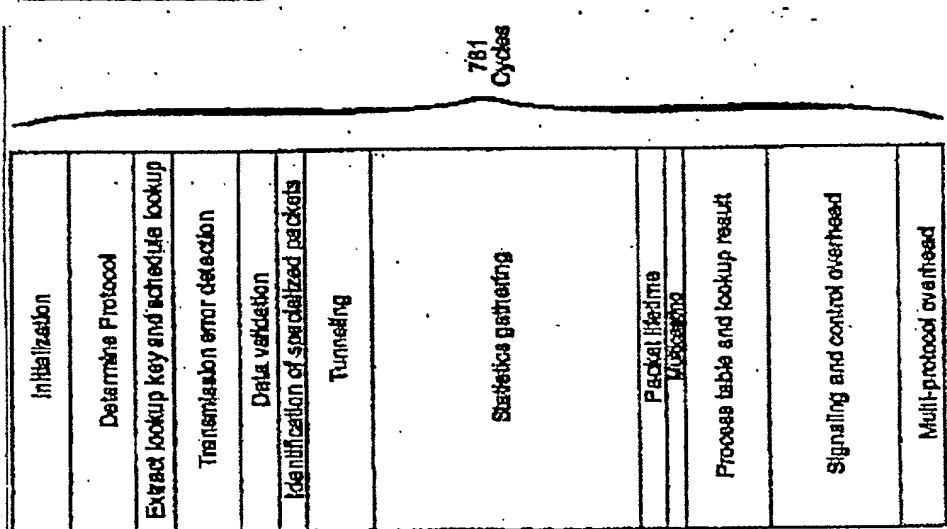


Figure 7 Cycle expenditure by function

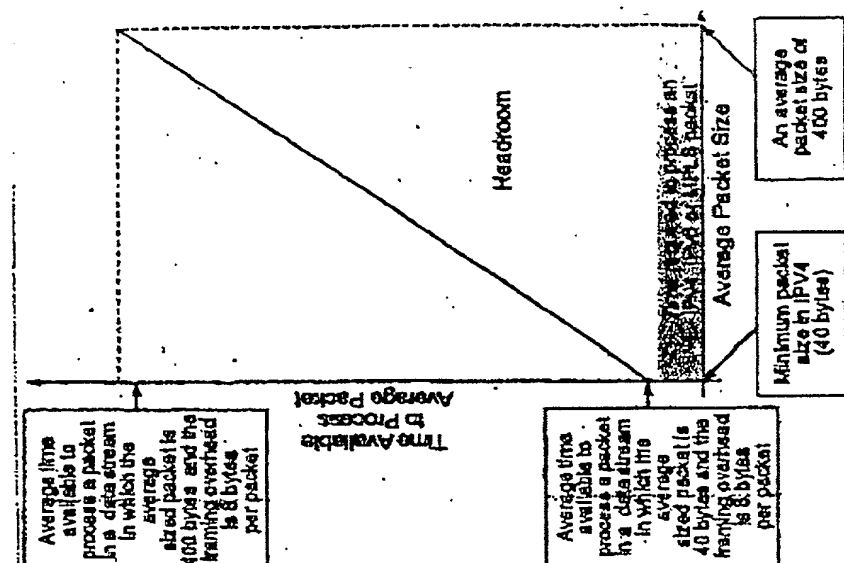


Figure 12 Headroom as a function of average packet size

Cumulative Distribution of Packet Sizes seen
at AIX from Sun Feb 20 16:01:51 to Sun Feb 27 13:59:18 2000

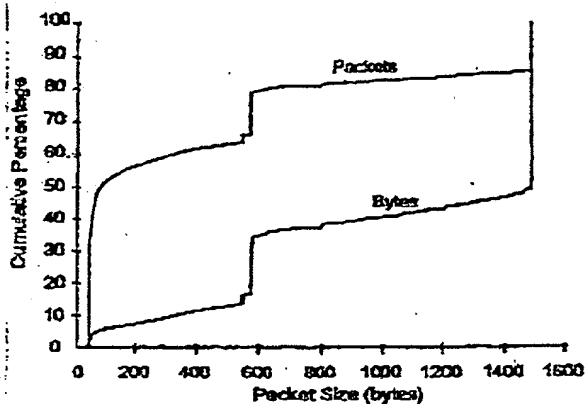


Figure 7 A real world traffic profile.

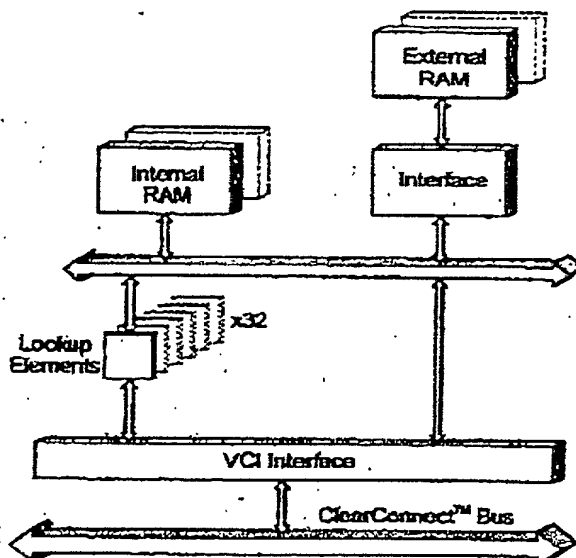


Figure 4 An example TLE

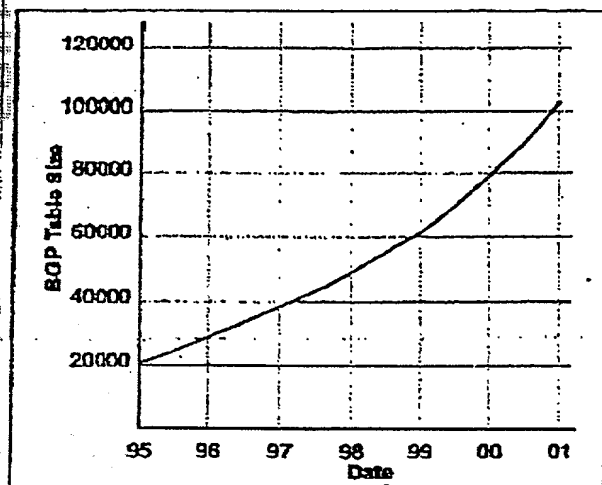


Figure 13 BGP Table Size

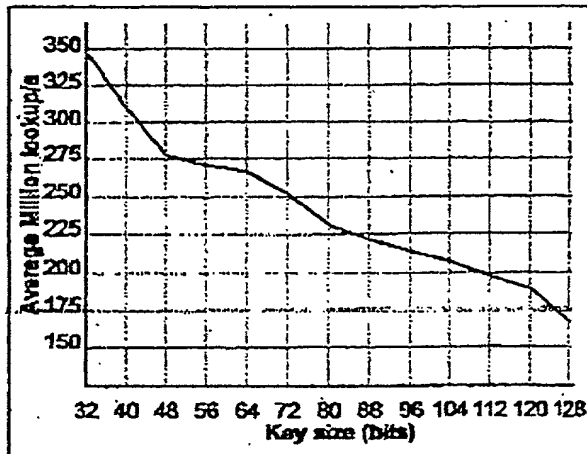


Figure 15 TLE Performance